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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/829,823	04/10/2001	Sameer I. Bidichandani	00CON104P	1553

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EXAMINER

PAN, DANIEL H

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/829,823

Applicant(s)

BIDICHANDANI ET AL.

Examiner

pan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 October 0804.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 June 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

1. Claims 1-32 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1,2,4,5, 10,11, 12, 13, 15, 16, 21,22, 23 are rejected under 35 U.S.C. 102(a) as being anticipated by Simar, Jr. et al. (6,182,203).

3. As to claims 1,2, 4,10, 12, 13, 21, 23, Simar disclosed a VLIW system as claimed comprising at least :

- a) identifying an instruction loop [instruction execute packet] having a plurality of instructions (see the execute packet k, k+1, k+2, k+3 etc.);
- 2) fetching the plurality of instructions from a program memory (e.g. see the fetch packet included the execute packets in fig.24, col.33, lines 46-60, col.34, lines 36-40, see also each execute packet included up to 8 instructions for background teaching);
- 3) storing the plurality of instructions into a storage (not explicitly shown, e.g. see fig.24, see also fig.1 [fetch unit], col.14, lines 34-56);
- d) determining the processor required to execute the plurality of instructions (e.g. see the determination of whether to dispatch of the instructions for execution was released in col.23, lines 24-45);

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e) outputting the instructions for execution and executed instructions (see the dispatch of the instructions for execution in col.23, lines 24-45).;

f) tracking module for tracking the desired instruction in the instruction packet and output the desired instruction for execution (e.g. see the p bit for indicating the instruction execution in col.14, lines 34-56, see also the dispatch of the instructions in 34, lines 36-59).

4. Simar did not specifically show a queue as claimed. However, Simar's instruction packet must have a storage or queue to hold the instructions for purpose of fetching in the fetch unit because each instruction had a least bit position for indicating the execution concurrency (e.g. see col.33, lines 46-58, col.34, lines 40-49), and without a storage for holding the instruction packets, the determination of concurrent execution would not be possible, therefore, the Simar must have a queue or the like in the fetch unit for storing the instructions to be dispatched for execution. And, since no specific type of queue is being recited in the claim, therefore, any storage which holds the instructions should be applicable.

5. As to claims 5,16, as to the limitation of the checking of the PC value, Simar also included the checking of pc value (e.g. see col.38, lines 23-28).

6. AS to claims 11,22, Simar also showed external memory (see the external memory interface in col.6, lines 36-37).

7. As to claim 15, see the current execute packet I col.34, lines 55-66).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 3,6-9, 14, 17-20, 24-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Simar, Jr. et al. (6,182, 203) in view of Wing et al. (5,926,832) .

9. As to claims 3,6-9, 14, 17-20, 24, 27-30, limitations of the parent claims have been discussed in the previous paragraph, therefore, it will not be repeated herein.

Simar did not specifically show the head pointer or the access pointer for the selected register in a queue as claimed. However, Wing disclosed a head pointer used in a queue (col.17, lines 1-20). It would have been obvious to one of ordinary skill in the art at the time of the claimed invention was made to use Wing in Simar for including the head pointer in the queue as claimed because the use of Wing could provide more flexible selection registers based on specific length of the instruction length, and it could be readily done by configuring the queue pointer of Wing into Simar with a modified control variables such as read and write heads of the specific queue , thereby providing flexible control over the selected instruction registers, and because Simar did disclosed that his instruction execute packets could vary in size and the

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variable length was a key for saving memory size (e.g. see col.33, lines 55-61), which was a suggestion for of the need of including the queue pointer to adapt to the variable length for the purpose of saving the memory, and in doing so, provided a motivation.

10. AS to claim 25, see the current execute packet I col.34, lines 55-66).

11. As to claim 26, as to the limitation of the checking of the PC value, Simar also included the checking of pc value (e.g. see col.38, lines 23-28).

12. As to claim 31, Simar also taught a cache in see col.34, line 38.

13. As to claim 32, Simar also showed external memory (see the external memory interface in col.6, lines 36-37).

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Babaian et al. (5,794,029) is cited for the teaching of the VLIW loop (e.g. see fig.3, col.12, lines 12-29).

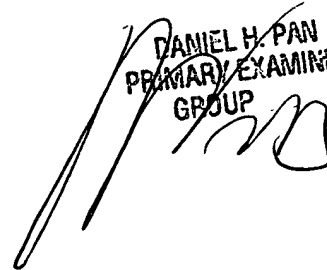
b) Tremblay et al. (6,314,509) is cited for the teaching of the instruction groups with the associated queue (e.g. see col.10, lines 21-57).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696.

The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


DANIEL H. PAN
PRIMARY EXAMINER
GROUP